ATTACHED ARE:

1) A transcribed copy of BAA 99-03 as it appeared in the *Commerce Business Daily* (CBD) of October 20, 1998 and

2) the BAA 99-03 Proposer Information Pamphlet.

Due to the possibility of transcription errors, the official CBD announcement takes precedence over this transcription in any disagreement between the two. The transcription is provided for your convenience only.

DATA INTENSIVE SYSTEMS SOL BAA 99-03 DUE 12/04/98 POC Dr. José L. Muñoz, DARPA/ITO, Fax: (703) 522-7161 WEB: http://www.ito.darpa.mil. E-MAIL: baa99-03@darpa.mil.

The Defense Advanced Research Projects Agency (DARPA) often selects its research efforts through the Broad Agency Announcement (BAA) process. The BAA will appear first in the Commerce Business Daily, published by the U.S. Government, Department of Commerce. The following information is for those wishing to respond to the Broad Agency Announcement.

The purpose of the Data Intensive Systems (DIS) program is to develop a new memory architecture for computing systems that allows "data-starved" applications to run up to two to three orders-of-magnitude faster than they will on contemporary virtual memory systems. The new memory architecture will allow these applications to manage the placement and flow of their data. In addition, applications will be able to manipulate data in the memory subsystem itself.

The performance of many Defense applications, for example model-based ATR, will be constrained not by the processing speed or memory but rather by the ability of their memory systems to deliver the data in a timely fashion. Similarly there are instances of object-oriented database systems where the processors are idle for 90+% of the time.

Major challenges facing data-starved applications are inadequate memory bandwidth and sub-optimal use of cache (high speed memory) to do complicated (i.e. irregular) memory access patterns. To address these problems applications must be able to manipulate data within the memory itself and control the movement of data within the memory hierarchy.

The DIS program solicits research to define, develop and accelerate the adoption of a new class of computing, memory, cache and I/O sub-systems. The DIS program will produce a hybrid computing/memory system that to the naive user will appear to be a standard COTS computer, complete with all of the COTS software products normally associated with such machines. However, it will also allow application programmers to choreograph the movement of data within the memory hierarchy in addition to enable

applications to process the data in-place when appropriate. This will allow new applications, for example Dynamic Databases, to begin with existing software products and then evolve them to perform orders-of-magnitude faster by exploiting this intelligent memory hierarchy.

Of particular interest to this solicitation are the following technical topic areas:

1. Intelligent DRAM memories: DRAM memories which contain an instruction processing capability that is programmable, enabling a new programming model where some of the program is sent to the data;
2. Smart caches: Configurable caches that would enable applications to precisely control the movement and placement of their data within the memory hierarchy;
3. Clever devices: Logic at the I/O devices and sensors that would enable applications to execute logic down at the device or sensor.
4. Algorithmic techniques that exploit these new technologies and enable them to be efficiently and effectively utilized;
5. Applications and demonstrations incorporating currently available, or soon to be available, logic-in-memory devices.
6. Other DIS areas: Topics are not limited to those listed above, but proposals should be for research that substantially contributes towards the DIS goals stated.

PROGRAM SCOPE:

Proposed research should investigate innovative approaches and techniques that lead to or enable revolutionary advances in the state-of-the-art. Proposals are not limited to the specific strategies listed above and alternative visions will be considered. However, proposals should be for research that substantially contributes towards the goals stated. Research should result in prototype hardware and/or software demonstrating integrated concepts and approaches. Specifically excluded is research that primarily results in evolutionary improvement to the existing state of practice or focuses on a specific system or solution. Integrated solution sets embodying significant technological advances are strongly encouraged over narrowly defined research endeavors. Proposals may involve other research groups or industrial cooperation and cost sharing.

GENERAL INFORMATION:

Proposers must submit an original and nine (9) copies of full proposals in time to reach DARPA by 4:00 PM (ET), Friday, December 4, 1998, in order to be considered. Proposers must obtain a pamphlet, BAA 99-03 Proposer Information, which provides further information on the areas of interest, submission, evaluation, funding processes, and full proposal formats. This pamphlet may be obtained by fax, electronic mail, or mail request to the administrative contact address given below, as well as at URL address http://www.ito.darpa.mil/Solicitations.html. Proposals not meeting the format described in the pamphlet may not be reviewed. This Commerce Business Daily notice, in conjunction with the pamphlet BAA 99-03 Proposer Information, constitutes the total BAA. No additional information is available, nor will a formal RFP or other

solicitation regarding this announcement be issued. Requests for same will be disregarded.

The Government reserves the right to select for award all, some, or none of the proposals received.

All responsible sources capable of satisfying the Government's needs may submit a proposal that shall be considered by DARPA. Historically Black Colleges and Universities (HBCU) and Minority Institutions (MI) are encouraged to submit proposals and join others in submitting proposals. However, no portion of this BAA will be set aside for HBCU and MI participation due to the impracticality of reserving discrete or severable areas of this research for exclusive competition among these entities. Evaluation of proposals will be accomplished through a scientific review of each proposal using the following criteria, which are listed in descending order of relative importance:
(1) overall scientific and technical merit,
(2) potential contribution and relevance to DARPA mission,
(3) offeror's capabilities and related experience,
(4) plans and capability to accomplish technology transition, and
(5) cost realism.

All administrative correspondence and questions on this solicitation, including requests for information on how to submit a proposal to this BAA, must be directed to one of the administrative addresses below by 4:00 PM (ET), Friday, November 27, 1998; e-mail or fax is preferred. DARPA intends to use electronic mail and fax for some of the correspondence regarding BAA 99-03. Proposals may not be submitted by fax; any so sent will be disregarded.

The administrative addresses for this BAA are:

Fax: 703-522-7161 Addressed to: DARPA/ITO, BAA 99-03,
Electronic Mail: baa99-03@darpa.mil,
Electronic File Retrieval: http://www.ito.darpa.mil/Solicitations.html,
Mail: DARPA/ITO,
ATTN: BAA 99-03,
3701 North Fairfax Drive,
Arlington, VA 22203-1714.

Posted 10/16/98 (W-SN262885). (0289)

SPONSOR: Defense Advanced Research Projects Agency (DARPA), Contract Management Directorate (CMD), 3701 N. Fairfax Dr., Arlington, VA 22203-1714

SUBFILE: PSE (U.S. GOVERNMENT PROCUREMENTS, SERVICES)
SECTION HEADING: A Research and Development
PUBLICATION DATE: OCTOBER 20, 1998

ISSUE: PSA-2204

BAA 99-03 PROPOSER INFORMATION PAMPHLET

The Defense Advanced Research Projects Agency (DARPA) often selects its research efforts through the Broad Agency Announcement (BAA) process. The BAA will appear first in the *Commerce Business Daily*, published by the U.S. Government, Department of Commerce. The following information is for those wishing to respond to the Broad Agency Announcement.

DATA INTENSIVE SYSTEMS SOL BAA 99-03 DUE 12/4/1998 Dr. José L. Muñoz, DARPA/ITO, FAX: (703) 522-7161

The purpose of the Data Intensive Systems (DIS) program is to develop a new memory architecture for computing systems that allows "data-starved" applications to run up to two to three orders-of-magnitude faster than they will on contemporary virtual memory systems. The new memory architecture will allow these applications to manage the placement and flow of their data. In addition, applications will be able to manipulate data in the memory subsystem itself.

The performance of many Defense applications, for example model-based ATR, will be constrained not by the processing speed or memory but rather by the ability of their memory systems to deliver the data in a timely fashion. Similarly there are instances of object-oriented database systems where the processors are idle for 90+% of the time.

Major challenges facing data-starved applications are inadequate memory bandwidth and sub-optimal use of cache (high speed memory) to do complicated (i.e. irregular) memory access patterns. To address these problems applications must be able to manipulate data within the memory itself and control the movement of data within the memory hierarchy.

The DIS program solicits research to define, develop and accelerate the adoption of a new class of computing, memory, cache and I/O sub-systems. The DIS program will produce a hybrid computing/memory system that to the naïve user will appear to be a standard COTS computer, complete with all of the COTS software products normally associated with such machines. However, it will also allow application programmers to choreograph the movement of data within the memory hierarchy in addition to enable applications to process the data in-place when appropriate. This will allow new applications, for example Dynamic Databases, to begin with existing software products and then evolve them to perform orders-of-magnitude faster by exploiting this intelligent memory hierarchy.

Of particular interest to this solicitation are the following technical topic areas:

1. Intelligent DRAM memories: DRAM memories which contain an instruction processing capability that is programmable, enabling a new programming model where some of the program is sent to the data;

2. Smart caches: Configurable caches that would enable applications to precisely control the movement and placement of their data within the memory hierarchy;
3. Clever devices: Logic at the I/O devices and sensors that would enable applications to execute logic down at the device or sensor.
4. Algorithmic techniques that exploit these new technologies and enable them to be efficiently and effectively utilized;
5. Applications and demonstrations incorporating currently available, or soon to be available, logic-in-memory devices.
6. Other DIS areas: Topics are not limited to those listed above, but proposals should be for research that substantially contributes towards the DIS goals stated.

(1) INTELLIGENT MEMORIES: It is now technically feasible to integrate processors and DRAM memories on the same die. One could then consider a new programming paradigm where some of the application instructions are sent to the data, as opposed to the conventional method of sending the data to the application. These intelligent DRAM memories would also be able to emulate content-addressable memory; execute garbage collection and data compression transparently; and enable object-oriented methods to execute in place. DARPA solicits proposals to design an appropriate architecture for such an intelligent memory and to prototype and demonstrate it as an enhancement to the memory of a standard computing system. Research in this technology topic area requires that processor instruction set design, compiler and operating systems activities be addressed to facilitate a demonstration.

(2) SMART CACHES: Databases and large Defense applications access data in patterns that defeat the caching mechanisms in conventional VM computers. Specific examples include chasing pointers in Object Oriented codes, computing FFTs in signal processing programs, and processing sparse matrices in engineering applications. The movement of data within the memory subsystems of today's computers is managed by operating systems and hardwired state machines. Even if programmers and compilers are able to determine a preferred access pattern of data movement, they are unable to execute this preferred behavior as no mechanisms exist enabling them to do so.

This technical topic area will address this problem by developing mechanisms that allow applications to directly manage the flow of data throughout the memory hierarchy. Such memory hierarchies must support full-bandwidth access to data gathered from, or scattered to, memory in accordance with address patterns generated by the application or indicated by a compiler.

(3) CLEVER DEVICES: Many data-intensive applications could benefit by a modicum of logic at the I/O device or the sensor. For example, an application that has complete control of a disc could execute a more intelligent data layout for subsequent retrieval or perform application optimal head/seek operations. Examples at a sensor would be to perform data conversion, data packing/unpacking operations, gain control or early signal processing functions such as FFT.

To address this area, proposals are sought for prototype demonstrations exploring an appropriate instruction set for these devices in addition to the programming paradigm that would be used at the application and/or operating system driver level that would enable an application to control these devices.

Successful proposals in this area must address the multi-user/multi-tasking nature (e.g. enforcement of protection boundaries) of many of the devices to which this technology will be applied.

(4) ALGORITHMIC TECHNIQUES: This technical topic area is looking to explore algorithmic techniques that explicitly exploit the capabilities of the novel components developed within the DIS program. Of particular interest are those techniques that both efficiently, i.e. from a performance perspective, and effectively, i.e. from a programming perspective, utilize these developing technologies.

What data structures are best suited? How should data be traversed? How to best convey various data reorganization requirements (e.g. corner-turning)? Are there sufficient control techniques in programming languages to handle this new newly enabled paradigm? When should instructions be executed in memory vs. moving the data up the hierarchy to the CPU?

One goal of the program is that the technology being developed by this program be transparent to legacy software. That is, that the compilers handle any of the effort required to utilize these intelligent memories and/or caches (perhaps with some additional information provided). Therefore, new algorithms that could be synthesized using modern compiler designs are of special interest; i.e. how might the innovative algorithmic approaches be eventually embedded within the compiler infrastructure.

Successful proposers to this topic area will be expected to prototype and evaluate their algorithms within the context of specific DIS hardware designs. Reference should be made to http://www.darpa.mil/ito/research/dis/index.html for a description of efforts under the DIS program.

(5) APPLICATIONS AND DEMONSTRATIONS: There exists, or will soon exist, commercial parts supporting the processor-in-memory architecture and/or FPGA-in-memory. This topic area solicits proposals and implementations of novel applications and/or system approaches using these components in innovative ways.

(6) OTHER ACS AREAS: Proposed research should investigate innovative approaches and techniques that lead to or enable revolutionary advances in the state-of-the-art. Topics are not limited to those listed above, but proposals should be for research that substantially contributes towards the goals stated. Research should result in prototype hardware/software demonstrating integrated concepts and approaches.

PROGRAM SCOPE:

Proposed research should investigate innovative approaches and techniques that lead to or enable revolutionary advances in the state-of-the-art. Proposals are not limited to the specific strategies listed above and alternative visions will be considered. However, proposals should be for research that substantially contributes towards the goals stated. Research should result in prototype hardware and/or software demonstrating integrated concepts and approaches. Specifically excluded is research that primarily results in evolutionary improvement to the existing state of practice or focuses on a specific system or solution. Integrated solution sets embodying significant technological advances are strongly encouraged over narrowly defined research endeavors. Proposals may involve other research groups or industrial cooperation and cost sharing.

SUBMISSION PROCESS:

An original and nine (9) copies of each proposal must be submitted to the administrative address for this BAA in time to reach DARPA by 4:00 PM (ET) Friday, December 4, 1998, in order to be considered. DARPA will acknowledge receipt of submissions and assign control numbers that should be used in all further correspondence regarding proposals.

The typical proposal should express a consolidated effort in support of one or more technical topic areas. Disjoint efforts should not be included in a single proposal.

Restrictive notices notwithstanding, proposals may be handled, for administrative purposes only, by a support contractor. This support contractor is prohibited from competition in DARPA technical research and is bound by appropriate non-disclosure requirements.

EVALUATION AND FUNDING PROCESSES:

Proposals will not be evaluated against each other since they are not submitted in accordance with a common work statement. DARPA's intent is to review proposals as soon as possible after they arrive; however, proposals may be reviewed periodically for administrative reasons. For evaluation purposes, a proposal is the document described in PROPOSAL FORMAT Section I and Section II (see below). Other supporting or background materials submitted with the proposal will be considered for the reviewer's convenience only and not considered as part of the proposal.

Evaluation of proposals will be accomplished through a scientific review of each proposal using the following criteria, which are listed in descending order of relative importance:
(1) overall scientific and technical merit,
(2) potential contribution and relevance to DARPA mission,
(3) offeror's capabilities and related experience,

(4) plans and capability to accomplish technology transition, and
(5) cost realism.

It is anticipated that all proposals will be reviewed by Government officials and non-government personnel; however, contractors will not be used to conduct evaluations or analyses of any aspect of a proposal submitted under this BAA unless one of the three conditions identified in FAR 37.203(d) applies.

As soon as the proposal evaluation is completed, the proposer will be notified of selectability or non-selectability. Selectable proposals will be considered for funding; non-selectable proposals will be destroyed. (Copies of non-selectable proposals may be retained for filing purposes.) Not all proposals deemed selectable will be funded. Decisions to fund selectable proposals will be based on funds available, scientific and technical merit, and potential contribution and relevance to DARPA's mission and offeror's capabilities and expertise. DARPA may retain some selectable proposals for a period of up to one year in order to reconsider those proposals for funding. Submitters of those retained proposals will receive notification to that effect.

The Government reserves the right to select for award all, some, or none of the proposals received. Proposals identified for funding may result in a contract, grant, cooperative agreement, or other transaction depending upon the nature of the work proposed, the required degree of interaction between parties, and other factors. If warranted, portions of resulting awards may be segregated into pre-priced options.

GENERAL INFORMATION:

Proposals not meeting the format described in this pamphlet may not be reviewed. Proposals may not be submitted by fax; any so sent will be disregarded. The *Commerce Business Daily* notice, in conjunction with this pamphlet, BAA 99-03 Proposer Information, constitutes the total BAA. No additional information is available, nor will a formal RFP or other solicitation regarding this announcement be issued. Requests for same will be disregarded. All responsible sources capable of satisfying the Government's needs may submit a proposal that shall be considered by DARPA. Historically Black Colleges and Universities (HBCU) and Minority Institutions (MI) are encouraged to submit proposals and join others in submitting proposals. However, no portion of this BAA will be set aside for HBCU and MI participation due to the impracticality of reserving discrete or severable areas of this research for exclusive competition among these entities.

PROPOSAL FORMAT:

Proposals shall include the following sections, each starting on a new page (where a "page" is 8-1/2 by 11 inches with type not smaller than 12 point) and with text on one side only. The submission of other supporting materials along with the proposal is strongly discouraged. Sections I and II of the proposal shall not exceed 40 pages. Maximum page lengths for each section are shown in braces {} below.

Section I. Administrative

{1} Cover Page including: (1) BAA number; (2) Technical topic area; (3) Proposal title; (4) Technical point of contact including: name, telephone number, electronic mail address, fax (if available) and mailing address; (5) Administrative point of contact including: name, telephone number, electronic mail address, fax (if available) and mailing address; (6) Summary of the costs of the proposed research, including total base cost, estimates of base cost in each year of the effort, estimates of itemized options in each year of the effort, and cost sharing if relevant; and (7) Contractor's type of business, selected from among the following categories: "LARGE BUSINESS," "SMALL DISADVANTAGED BUSINESS," "OTHER SMALL BUSINESS," "HBCU," "MI," "OTHER EDUCATIONAL," or "OTHER NONPROFIT."

Section II. Detailed Proposal Information

This section provides the detailed discussion of the proposed work necessary to enable an in-depth review of the specific technical and managerial issues. Specific attention must be given to addressing both risk and payoff of the proposed work that make it desirable to DARPA.

A. {1} Innovative claims for the proposed research. This page is the centerpiece of the proposal and should succinctly describe the unique proposed contribution.

B. {18} Technical rationale, technical approach and constructive plan for accomplishment of technical goals in support of innovative claims and deliverables.

C. {2} Deliverables associated with the proposed research. Include in this section all proprietary claims to results, prototypes, or systems supporting and/or necessary for the use of the research, results, and/or prototype. If there are no proprietary claims, this should be stated. The offeror must submit a separate list of all technical data or computer software that will be furnished to the Government with other than unlimited rights (see DFARS 227.)

D. {3} Statement of Work (SOW) written in plain English, outlining the scope of the effort and citing specific tasks to be performed and specific contractor requirements.

E. {1} Schedule of milestones for the proposed research.

F. {2} Technology Transfer. Description of the transferable technology and expected technology transfer path.

G. {3} Comparison with other ongoing research indicating advantages and disadvantages of the proposed effort.

H. {3} List of key personnel, concise summary of their qualifications, and discussion of proposer's previous accomplishments and work in this or closely related research areas. Indicate the level of effort to be expended by each person during each contract year and other (current and proposed) major sources of support for them and/or commitments of their efforts. DARPA expects all key personnel associated with a proposal to make substantial time commitment to the proposed activity.

I. {1} Description of the facilities that would be used for the proposed effort.

J. {5} Cost by task, with breakdown into accounting categories and equipment for the entire contract and for each contract year. Where the effort consists of multiple portions that could reasonably be partitioned for purposes of funding, these should be identified as contract options with separate cost estimates for each. Details of any cost sharing should also be included. Budgets for Government furnished/funded equipment should be limited to experimental apparatus and exclude office and laboratory equipment normally associated with Information Technology research environments, such as servers, workstations, PCs, laptops, PDAs, routers, printers, copiers, fax machines, etc.

Awards made under this BAA may be subject to the provisions of the Federal Acquisition Regulation (FAR) Subpart 9.5, Organizational Conflict of Interest. All offerors and proposed subcontractors must affirmatively state whether they are supporting any DARPA technical office(s) through an active contract or subcontract. "Support contract" or "support contractor" includes a contract or subcontract for acquisition of System Engineering and Technical Assistance (SETA) services, and other support service contracts in which any one of the following situations apply: have personnel who regularly maintain offices or frequently occupy space within DARPA; maintain external spaces in which DARPA personnel maintain offices or frequently occupy; or have personnel with any access to the DARPA fiscal database, EIS, or contractual or programmatic documentation related to other than their own contact(s). All affirmations must state which office(s) the offeror supports, and identify the prime contract number. Affirmations should be furnished at the time of proposal submission. All facts relevant to the existence or potential existence of organizational conflicts of interest, as that term is defined in FAR 9.501, must be disclosed in Section II., H of the proposal, organized by task and year. This disclosure shall include a description of the action the Contractor has taken, or proposes to take, to avoid, neutralize, or mitigate such conflict.

Section III. Additional Information

A bibliography of relevant technical papers and research notes (published and unpublished) that document the technical ideas upon which the proposal is based. Copies of not more than three relevant papers may be included in the proposal submission; provide one set for the original proposal and one set for each of the nine (9) proposal copies. Please note: the materials listed in Section III. Additional Information, and submitted with the proposal, will be considered for the reviewer's convenience only and not considered as part of the proposal for evaluation purposes.

Additional Electronic Submission Encouraged

In ADDITION to the paper proposals, proposers are strongly encouraged to send ASCII text electronic copies of the statement of work and equipment needs to the following email address: baa99-03@darpa.mil. The title of the proposal and the name of the proposing organization must be provided as a header to enable administrative staff to match these electronic submissions with the full proposals. The statement of work and equipment budgets must be identical (except for format) to the statement of work in the full proposal.

The administrative addresses for this BAA are:

Fax: 703-522-7161 Addressed to: DARPA/ITO, BAA 99-03
Electronic Mail: baa99-03@darpa.mil
Electronic File Retrieval: http://www.ito.darpa.mil/Solicitations.html
Mail: DARPA/ITO
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3701 North Fairfax Drive
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